Application No.	Applicant(s)
10/786.867	STENFORT, ROSS
Examiner	Art Unit
Linh V Nauven	2819
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DETAILED ACTION

1. This office action is in response to application filed on 03/03/04. Claims 1-20 are pending on this application.

Allowable Subject Matter

- 2. Claims 1 20 are allowed.
- 3. The following is an examiner's statement of reasons for allowance:

With respect to claim 1, the prior art does not teach a method comprising:

defining a validity bit within a set of bits representing output data, the validity bit

indicating a status of the output data; defining a validity bit value pattern associated with
a particular data output frequency; assigning successive validity bit values of the validity
bit value pattern to the validity bit in accordance with each cycle of a clock signal;
transmitting the set of bits representing output data in accordance with each cycle of the
clock signal; and processing the output data according to the validity bit.

With respect to claim 8, the prior art does not teach a method for testing circuitry having a field programmable gate array (FPGA) and an application specific integrated circuit (ASIC), wherein the FPGA and ASIC have substantially similar logic; defining an FPGA validity bit pattern associated with a data output frequency; defining an ASIC validity bit pattern associated with the data output frequency; and operating the FPGA and the ASIC in accordance with their respective validity bit pattern to generate test results.

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With respect to claim 16, the prior art does not teach a frequency control module, comprising: a data rate control module configured to output a validity bit signal in accordance with a clock signal to be generated by a clock circuit; a logic stage configured to receive a data signal and the validity bit signal; and a transceiver connected to receive the data signal and the validity bit signal from the logic stage, the transceiver configured to recognize a valid state of the validity bit signal, the transceiver

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

defined to process the data signal in response to the valid state.

Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

Michael Tokar
Supervisory Patent Examiner
Technology Center 2800

Michael J. Tokan

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

LVN

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11/16/04